AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method of processing an input data word containing a plurality of abutting input data values, said method comprising ~~the steps of~~:

(i) performing one or more data processing operations upon said input data word and a further data word to generate an intermediate result data word containing a plurality of abutting intermediate result data values dependent upon said input data values and corresponding portions of said further data word, said one or more data processing operations being such that a corrupting result bit from a first result data value ~~may extend~~ extends into and ~~change~~ changes a value of a second result data value;

(ii) calculating an error correcting data word in dependence upon said input data word and said further data word, said error correcting data word having a value that represents any corrupting result bits that may be generated by said ~~step of~~ performing;

(iii) combining said intermediate result data word and said error correcting data word to remove ~~any~~ a change of value produced by a corrupting result bit and to generate an output data word, said output data word containing a plurality of abutting output data values being those ~~that would be~~ generated if said one or more data processing operations were performed upon said plurality input data values and said corresponding portions of said further data word in isolation from one another.

2. (Previously Presented) A method as claimed in claim 1, wherein said one or more data processing operations include an addition operation.

3. (Previously Presented) A method as claimed in claim 2, wherein said corrupting result bit is a lowest order bit of said first result data value changing a value of a highest order bit of said second result data value.

4. (Previously Presented) A method as claimed in claim 1, wherein said one or more data processing operations include a subtraction operation.

5. (Previously Presented) A method as claimed in claim 4, wherein said corrupting result bit is a lowest order bit of said first result data value changing a value of a highest order bit of said second result data value.

6. (Previously Presented) A method as claimed in claim 1, wherein said one or more data processing operations include a shift operation.

7. (Currently Amended) A method as claimed in claim 1, wherein said ~~step of~~ calculating includes performing an exclusive OR logical operation between said input data word and said further data word to generated an exclusive OR data word.

8. (Currently Amended) A method as claimed in claim 7, wherein said ~~step of~~ calculating includes performing an AND logical operation between said exclusive OR data word and a mask data word to generate said error correcting data word having bit values representing any corrupting result bits.

9. (Previously Presented) A method as claimed in claim 3, wherein said error correcting data word is subtracted from said intermediate result data word.

10. (Previously Presented) A method as claimed in claim 3, wherein said error correcting data word is added to said intermediate result data word.

11. (Currently Amended) A method as claimed in claim 9, wherein said ~~step of~~ combining includes shifting ~~said intermediate result data word~~ the result of claim 9 by one bit to divide said result data word by two.

12. (Previously Presented) A method as claimed in claim 1, wherein said input data values represent adjacent signal values within a stream of signal values being processed.

13. (Previously Presented) A method as claimed in claim 12, wherein said data values represent adjacent pixel values.

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14. (Currently Amended) A method as claimed in claim 1, wherein said input data values have an input data value bit-width and ~~may vary~~ are variable over a full range of values allowed by said input data value bit-width.

15. (Currently Amended) Apparatus for processing an input data word containing a plurality of abutting input data values, said apparatus comprising:

(i) processing logic operable to perform one or more data processing operations upon said input data word and a further data word to generate an intermediate result data word containing a plurality of abutting intermediate result data values dependent upon said input data values and corresponding portions of said further data word, said one or more data processing operations being such that a corrupting result bit

from a first result data value ~~may extend~~ extends into and change a value of a second result data value;

(ii) calculating logic operable to calculate an error correcting data word in dependence upon said input data word and said further data word, said error correcting data word having a value that represents any corrupting result bits ~~that may be~~ generated by said ~~step of performing~~ processing logic;

(iii) combining logic operable to combine said intermediate result data word and said error correcting data word to remove any change of value produced by a corrupting result bit and to generate an output data word, said output data word containing a plurality of abutting output data values being those ~~that would be~~ generated if said one or more data processing operations were performed upon said plurality input data values and said corresponding portions of said further data word in isolation from one another.

16. (Previously Presented) A computer program product including a computer program for controlling a data processing apparatus to perform data processing in accordance with a method as claimed in claim 1.